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Low Power And High Performance 32bit Unsigned Multiplier Using Adders

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Abstract

The Clutch Select Adder (CCA) provides a good compromise between cost and performance in clutch propagation adder design. However, conventional CCA is still area-consuming due to the dual ripple clutch adder (RCA) structure. In this paper, modification is done at gate-level to reduce area and power consumption. The Modified Clutch Select-Adder (MCCA) is designed for 8-bit, 16-bit, 32-bit and 64-bit and then compared with regular CCA respective architectures, and this MCCA is implemented in Booth Multiplier. This work evaluates the performance of the booth multiplier in terms of delay, area, power, and their products by implementing in Xilinx.

KEYWORDS– *Area-efficient, CCA, low power, Booth multiplier, RCA.*

1. Introduction

Addition is the heart of the arithmetic unit is often the work horse of a computational circuit. They are the necessary component of a data path, e.g. in microprocessors or a signal processor. In digital adders, the speed of addition is limited by the time required to propagate a clutch through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a clutch propagated into the next position.The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem.

In mobile electronics, reducing area and power consumption are key factors in increasing portability and battery life. Even in servers and desktop computers power dissipation is an important design constraint. Among various adders, the CCA is intermediate regarding speed and area.

We introduce Modified Clutch Select-Adder (MCCA) architecture to reduce area and power with minimum speed penalty .The MCCA is designed by using single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs.

2. 2. FUNCTION AND STRUCTURE OF BEC LOGIC

The basic work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CCA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CCA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function are shown in Figure1 and Table 1 respectively.

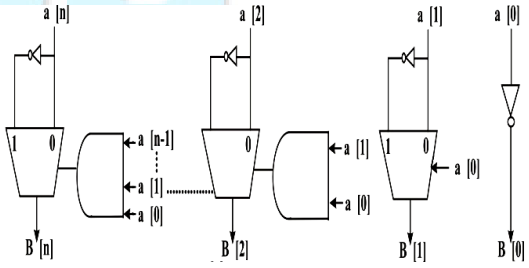


Figure. 1 4-Binary to excess-1 converter

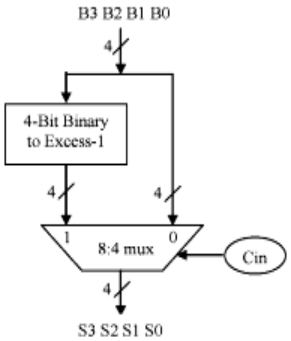
Table **1:** Function table of the 4-bit BEC

A[3:0]	B[3:0]
0000 0001 . . . . 1110 1111	0001 0010 . . . . 1111 0000

Figure. 2 4-b BEC with 8:4 mux

3. REGULAR CLUTCH SELECTADDER (RCCA)

A 16-bit clutch select has two types of block size namely uniform block size and variable block size. A 16-bit clutch select adder with a uniform block size has the delay of four full adder delays and three MUX delays. While a 16-bit clutch select adder with variable block size has the delay of two full adder delays, and four mux delays. Therefore we use 16-bit clutch select adder with variable block size. Ripple-clutch adders are the simplest and most compact full adders, but their performance is limited by a clutch that must ripple from the least-significant to the most-significant bit. A clutch-select adder achieves speeds 40% to 90% faster by performing additions in parallel and reducing the maximum clutch path.



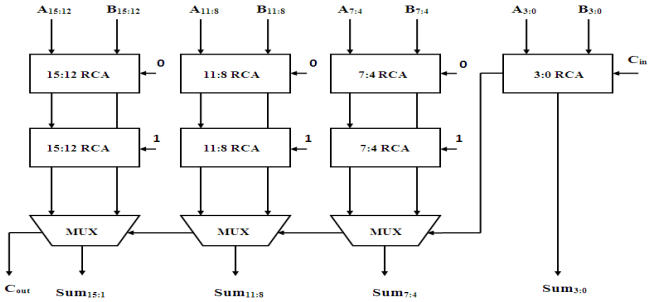


Figure 3 16-bit Conventional CCA

A clutch-select adder is divided into sectors, each of which, except for the least significant performs two additions in parallel, one assuming a clutch-in of zero, the other a clutch-in of one within the sector, there are two 4-bit ripple- clutch adders receiving the same data inputs but different Cin. The upper adder has a clutch-in of zero, the lower adder a clutch-in of one. The actual Cin from the preceding sector selects one of the two adders. If the clutch-in is zero, the sum and clutch-out of the upper adder are selected. If the clutch-in is one, the sum and clutch-out of the lower adder are selected. Logically, the result is not different if a single ripple-clutch adder were used. First the coding for full adder and different multiplexers of 6:3, 8:4, 10:5, and 12:6 was done. Then 2, 3, 4, 5-bit ripple clutch adder was done by calling the full adder. The 64-bit regular CCA was created by calling the ripple clutch adders and all multiplexers based on circuit.

4.MODIFIED CLUTCH SELECTADDER

A Modified Clutch Select-Adder (MCCA) design is proposed, which make use of single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. As the base of proposed design is that the number of logic gates used in BEC is less than that of RCA. Thus BEC replaces the RCA with Cin=1 instead of using dual RCAs to reduce area and power consumption of the conventional CCA. To replace the N-bit RCA, an N+1 bit BEC is required.The MCCA architecture for 16-bit is shown in Figure 4.The importance of BEC logic comes from the large silicon area reduction when designing MCCA for large number of bits.

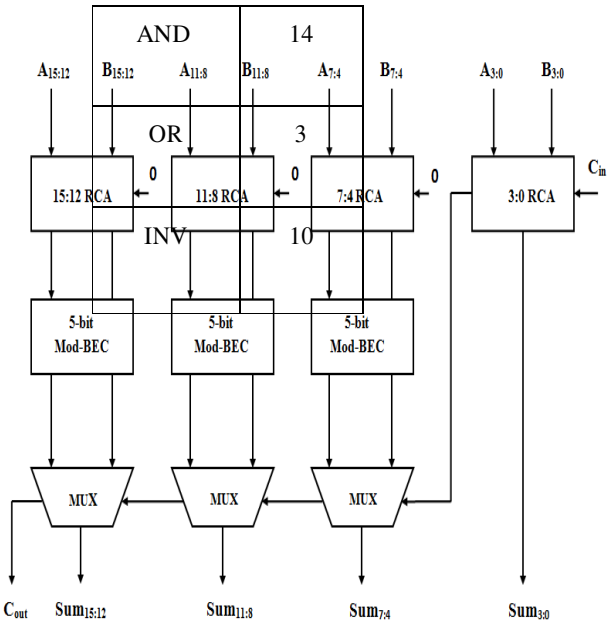


Figure. 4 16-bit Modified Clutch Select Adder

To elaborate this, the gate calculations are made for 4-bit BEC and 4-bit RCA area as under.

4.1 For 4-bit RCA

In 4-bit RCA, four FAs are connected in a chain. Therefore the gates require to built 4-bit RCA are shown in Table 2.

Table 2: AND, OR and INV gates in 4-bit RCA

AND	28
OR	16
INV	16

Table 3: AND, OR & INV gates in 4-bit BEC

5. IMPLEMENTATION IN BOOTH MULTIPLIER

Generally the booth multiplier consists of booth encoder/decoder, partial product generator and CCA. The CCA in booth multiplier uses multiple pairs of RCA so its area is not efficient, partial product generator is used to produce the partial product bits with the help of booth encoder output and Y-inputs, here the Wallace tree is the way of summing the partial product bits in parallel. the modified CCA is implemented in a 8 × 8 bit booth multiplier to achieve the final addition, in order to increase the efficiency of the booth multiplier. The delay time and area of modified booth multiplier is greatly reduced when we use the modified CCA. The structure of a modified booth multiplier is shown in fig.5. This architecture is more efficient than the conventional one in terms of area and power. Therefore, Booth multiplier architecture is low area, power, simple and efficient for VLSI hardware implementation.

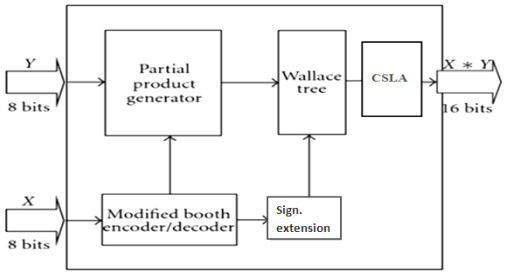


Figure 5 BoothMultiplier

6. OUTCOMES

The booth multiplier is designed using Verilog language and all the simulations are performed using model sim and implementations are done by Xilinx ISim simulator. The performance of booth multiplier is analysed and compared against the booth multiplier with RCCA designs. The number of gates used in the design indicates the area of design. The power consumption is measured in terms of total power and dynamic power. It can be seen from Table 4 that area and power consumption of MCCA is less than that of RCCA, table 6 shows the area and reduction percentage of the booth multiplier. Fig.6 shows the simulation output for the booth multiplier.

Table 4 : Comparison of area, power and speed of Conventional and Modified CCA

Design		Area (No. Of gates)	Power (in mW)
RCCA	8-bit	543	40
	16-bit	1103	43
	32-bit	2265	46
	64-bit	4643	57
MCCA	8-bit	378	39
	16-bit	762	41
	32-bit	1548	43
	64-bit	3174	50

Table 5: Reduction Percentage of Area, Power And Speed of Modified CCA

Word-size of Adder	Area Reduction (in Percent)	Power Consumption reduction(in %)
8-bit	16.5	8
16-bit	20.62	14
32-bit	22.21	16
64-bit	22.92	17

Table 6: Comparison of Conventional and Modified Booth Multiplier

Booth multiplier	Using RCCA	Using MCCA
No. of gates	4717	129
Power in (mW)	53	49

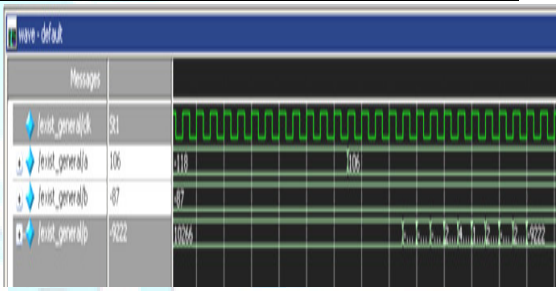


Fig 6 simulation result for booth multiplier using MCCA

7.Conclusion

A Modified Clutch Select-Adder (MCCA) is designed by using single Ripple Clutch Adders (RCA) and Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The MCCA architecture for 8-bit, 16-bit, 32-bit and 64-bit is designed and then compared with RCCA respective architectures. The MCCA is implemented in booth multiplier which reduces the area and power by 33.66% and 7.54% respectively. The syntheses are done by using Xilinx ISE.

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